


**TM05N50D**

**N-Channel Enhancement Mosfet**

<p><b>General Description</b></p> <ul style="list-style-type: none"> <li>• Low <math>R_{DS(ON)}</math></li> <li>• RoHS and Halogen-Free Compliant</li> </ul> <p><b>Applications</b></p> <ul style="list-style-type: none"> <li>• Load switch</li> <li>• PWM</li> </ul>	<p><b>General Features</b></p> <p><math>V_{DS} = 500V</math> <math>I_D = 5.0A</math>  <math>R_{DS(ON)} = 1.35\Omega(\text{typ.})@V_{GS} = 10V</math></p> <p>100% UIS Tested              100% <math>R_g</math> Tested</p> 
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**D:TO-252-3L**

Marking: 05N50

**Absolute Maximum Ratings** ( $T_A = 25^\circ C$  Unless Otherwise Noted)

Symbol	Parameter	Rating	Units	
$V_{DSS}$	Drain-Source Voltage	500	V	
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V	
$I_D$	Continuous Drain Current	$T_C = 25^\circ C$	5	A
		$T_C = 100^\circ C$	3.4	A
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>	20	A	
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note2</sup>	90	mJ	
$P_D$	Power Dissipation	$T_C = 25^\circ C$	45	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.8	$^\circ C/W$	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60	$^\circ C/W$	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$	

**Electrical Characteristics** ( $T_C=25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	500	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500V,$ $V_{GS} = 0V, T_J = 25^\circ\text{C}$	-	-	1	$\mu A$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 30V$	-	-	$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance <small>note3</small>	$V_{GS} = 10V, I_D = 2.5A$	-	1.35	1.6	$\Omega$
$C_{iss}$	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	-	462	-	pF
$C_{oss}$	Output Capacitance		-	54.2	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	8.8	-	pF
$Q_g$	Total Gate Charge	$V_{DD} = 400V, I_D = 5A,$ $V_{GS} = 10V$	-	13.5	-	nC
$Q_{gs}$	Gate-Source Charge		-	2	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	6	-	nC
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250V, I_D = 5A,$ $R_G = 25\Omega$	-	10	-	ns
$t_r$	Turn-On Rise Time		-	25	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	40	-	ns
$t_f$	Turn-Off Fall Time		-	52	-	ns
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	5	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	20	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0V, I_{SD} = 5A,$ $T_J = 25^\circ\text{C}$	-	-	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0V, I_S = 5A,$ $di/dt = 100A/\mu s$	-	220	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	3	-	$\mu C$

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $I_{AS} = 3A, V_{DD} = 50V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
3. Pulse Test: Pulse width  $\leq 300\mu s, \text{Duty Cycle } \leq 1\%$



Typical Performance Characteristics

Figure 1: Output Characteristics

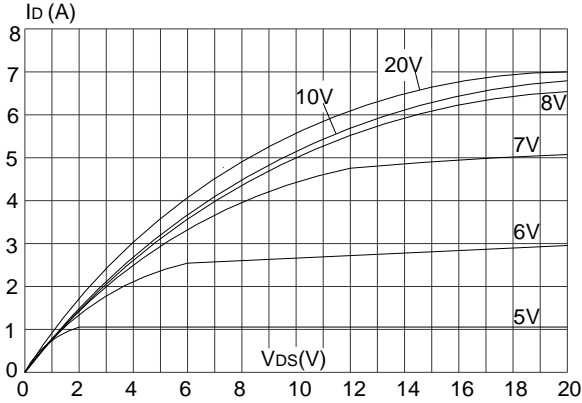


Figure 2: Typical Transfer Characteristics

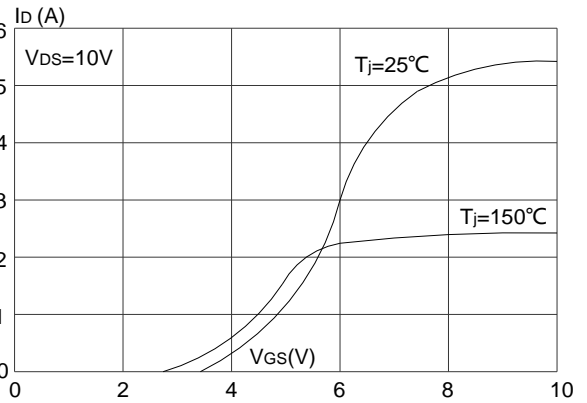


Figure 3: On-resistance vs. Drain Current

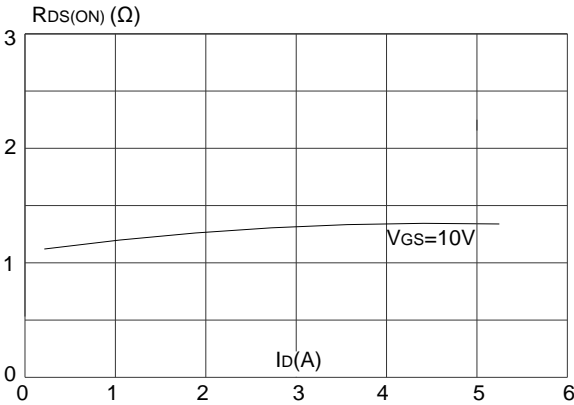


Figure 4: Body Diode Characteristics

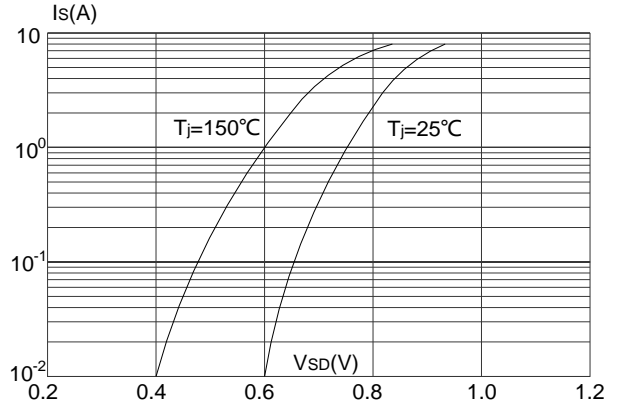


Figure 5: Gate Charge Characteristics

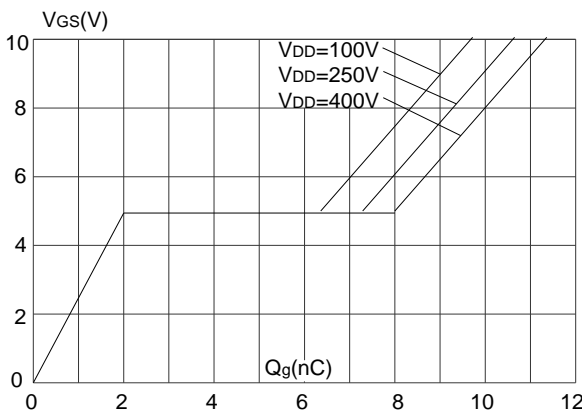
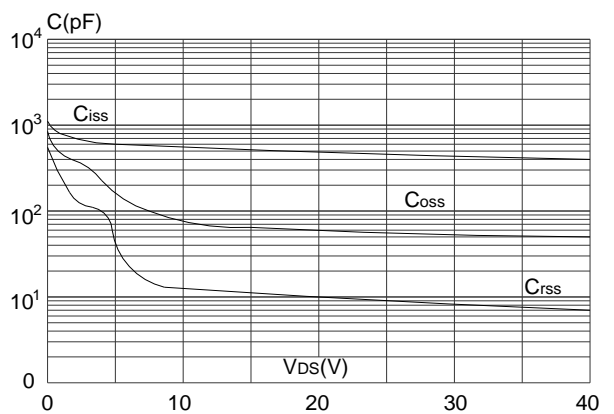


Figure 6: Capacitance Characteristics





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Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

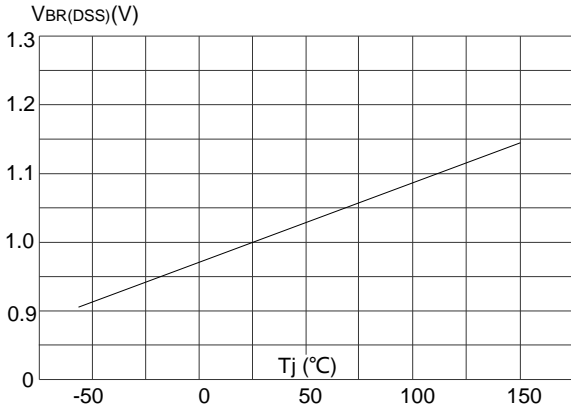


Figure 8: Normalized on Resistance vs. Junction Temperature

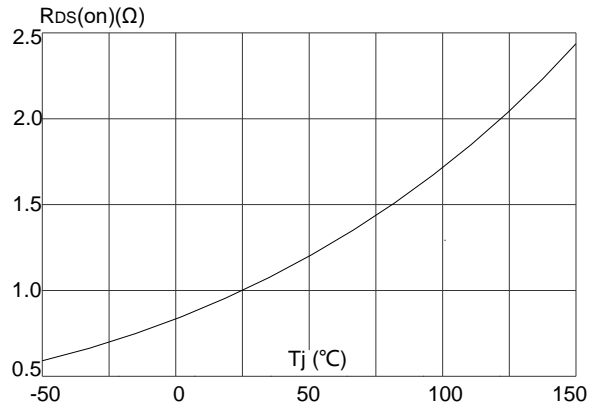


Figure 9: Maximum Safe Operating Area

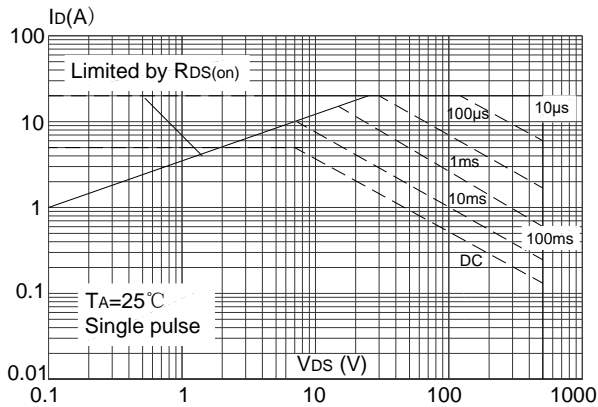


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

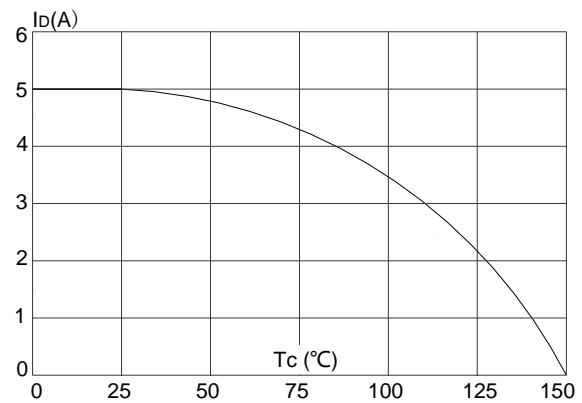


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220C, TO-251, TO-251S, TO-252)

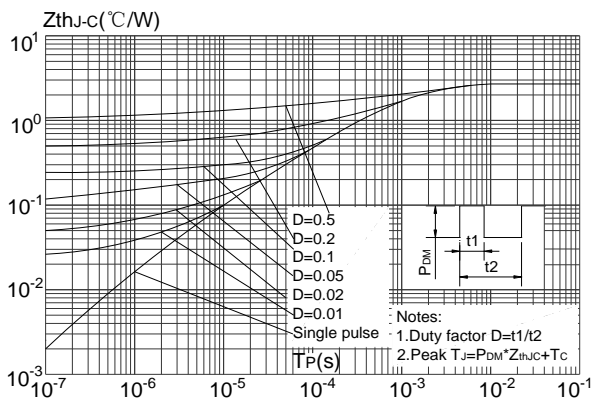
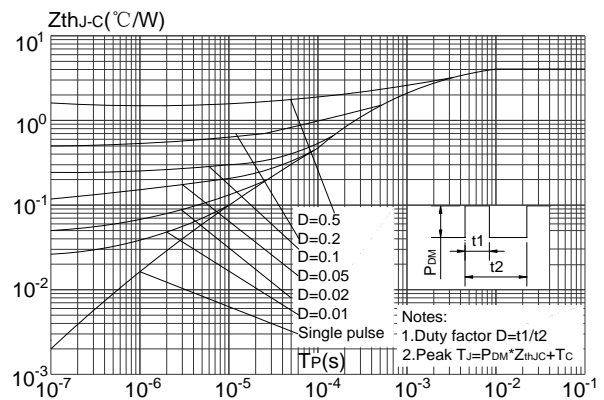


Figure.12: Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220F)





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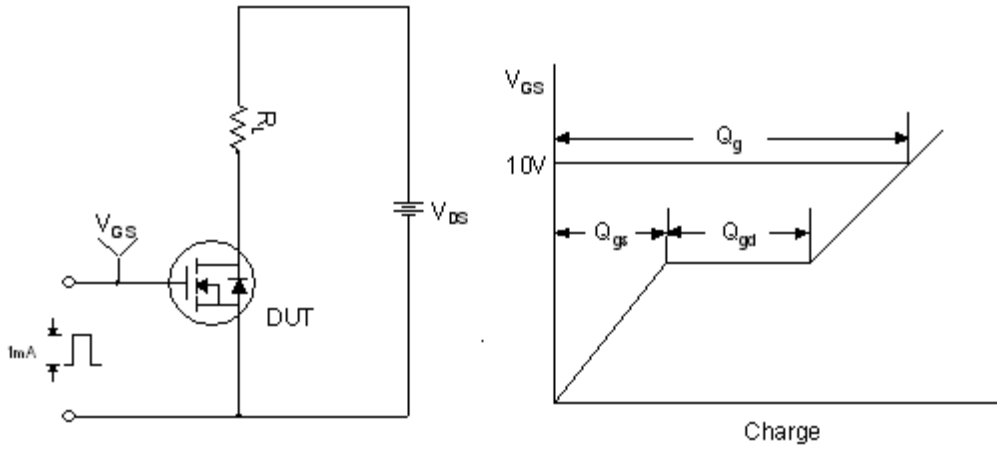


Figure 13. Gate Charge Test Circuit & Waveform

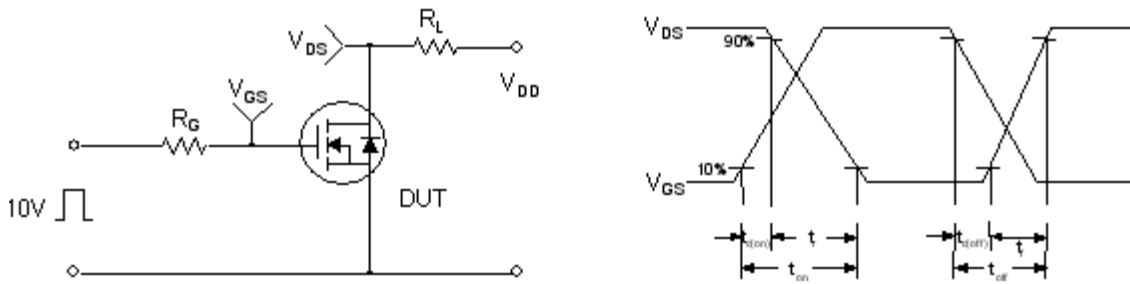


Figure 14. Resistive Switching Test Circuit & Waveforms

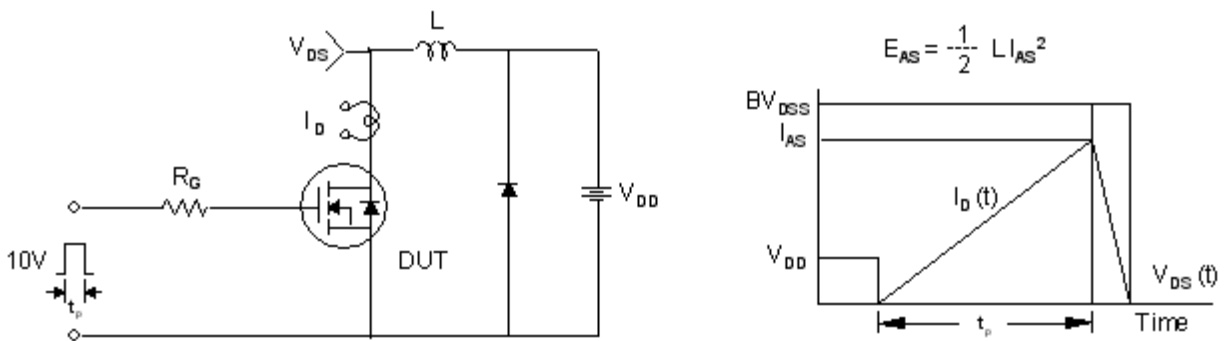
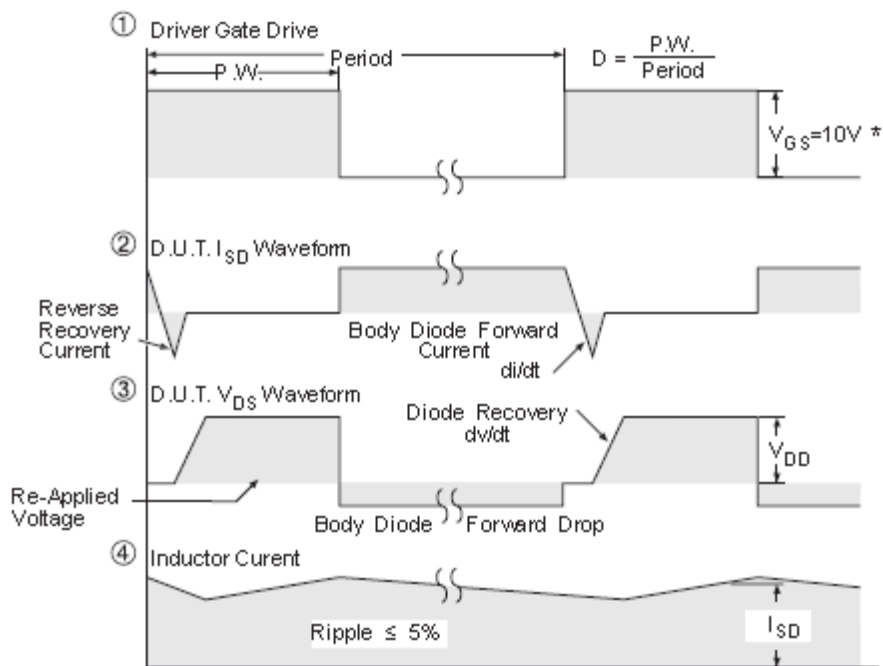
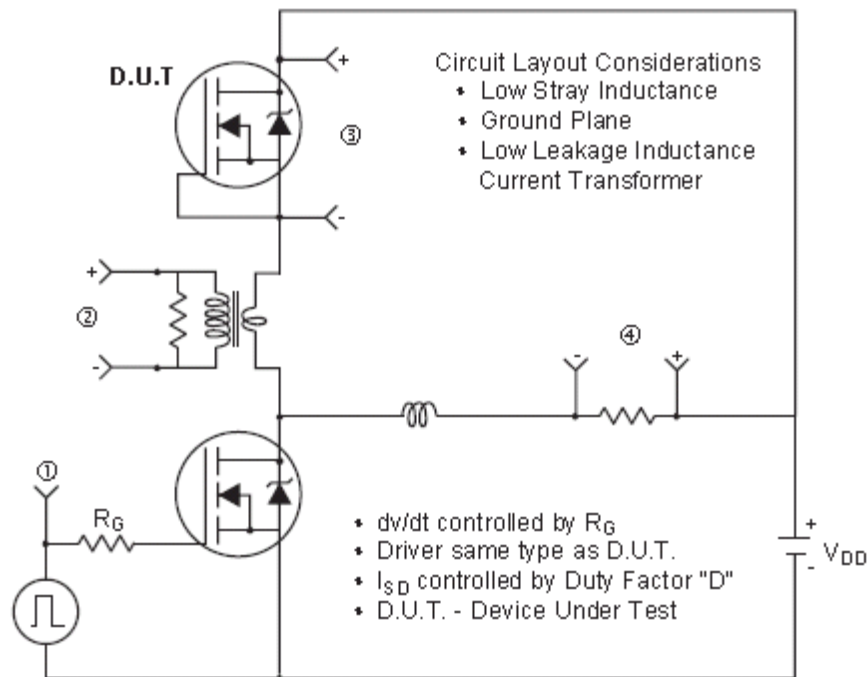


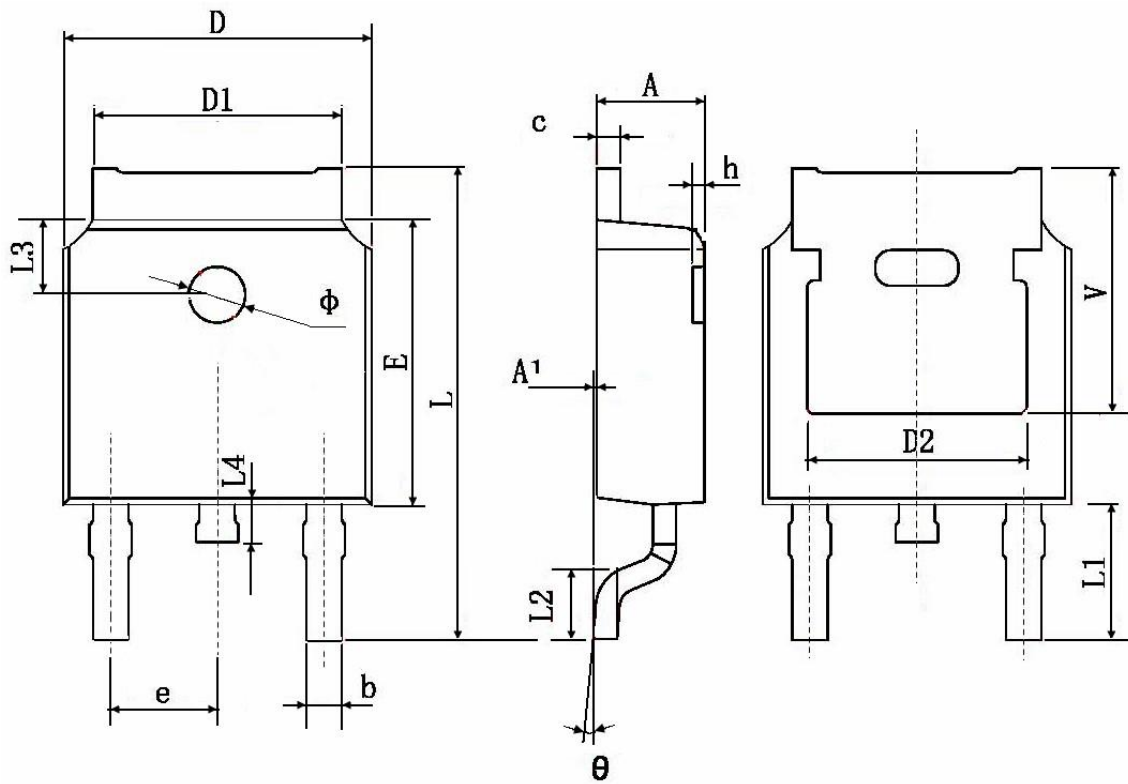
Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms



\*  $V_{GS} = 5V$  for Logic Level Devices

Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms (For N-channel)

## Package Information: TO-252-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	